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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,514	02/14/2002	Jeffrey P. Wright	500024.02	3185

7590 07/24/2003

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EXAMINER	
BUTLER, DENNIS	
ART UNIT	PAPER NUMBER
2185	11

DATE MAILED: 07/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	10/055,514	WRIGHT ET AL.	
	Examiner	Art Unit	
	Dennis M. Butler	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. This action is in response to amendment B received on March 26, 2003. Claims 1-72 are pending.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The amendments to claims 63 and 68 have not been entered because they do not comply with rule 1.173. The amendments have been addressed in this office action and these amendments will be entered if a proper after final amendment is submitted. However, any further improper amendments will be held non-responsive or will not be entered.

4. Applicant has submitted a stamped return receipt postcard as evidence that the original patent was submitted to the Office on October 30, 2002. The Office accepts applicant's evidence as proof applicant has submitted the original patent to the office. However, applicant is advised that the original patent is not present in applicant's application file and has been misplaced by the Office.

5. The rejection of claims 58, 59 and 61-72 under 35 USC 251 as being an improper recapture is withdrawn in view of applicant's arguments on pages 5-6 of amendment B.

6. The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following:

A) The declaration fails to contain a statement that **all** errors which are being corrected in the reissue application up to the time of filing of the oath/declaration arose without any deceptive intention on the part of the applicant. See 37 CFR 1.175 and

MPEP § 1414. The declaration states that "this error" arose without any deceptive intention.

B) The reference in the declaration to "the enclosed preliminary amendment" is improper because the preliminary amendment was not enclosed with the declaration. The preliminary amendment was received on February 14, 2002 while the declaration was received on June 14, 2002. Applicant is required to make accurate statements in the declaration. Correction is required.

C) Newly added claims 53-72 do not correct the identified error in the declaration. Claims 53-57 appear to be narrower than claim 43 in that they recite the pass gate and that the output node is coupled to ground. Claims 58-72 are directed to entirely different embodiments and do not merely eliminate the pass gate from claim 43 as described in the declaration. In addition, the declaration states that applicant's have the right to claim that "other means" may be used in the method for generating a pulse. However, applicant's have failed to describe what other means are being used, where there is support in the specifications for using other means and how the new claims correct the error by reciting the other means. Therefore, the declaration does not clearly identify an error that is being corrected by the reissue claims.

7. Claims 1-72 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

In the remarks, applicant requested that these rejections be held in abeyance until agreement of allowable subject matter. The rejections will not officially be held in abeyance. However, applicant may choose to not respond to these rejections until allowable subject matter is indicated. The rejection is maintained.

8. Claims 58 and 61-72 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Elements critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The specification describes the use of a pass gate to perform the steps of transferring and blocking the trigger signal from an input node to an output node, coupling and decoupling/deactivating the input node to the output node with figure 3, at column 4, lines 25-40 and at column 6, lines 29-39. No other methods of performing the above steps are described in the specification. In addition, applicant has distinguished the invention over the described prior art method by using a pass gate rather than the logic gate in the circuit of figure 1. Applicant describes the advantages of using a pass gate over the prior art circuitry at column 6, lines 29-39. This is clear evidence that the passgate is a critical element because applicant's pulse generating circuit generates the prior art pulse using a passgate circuit rather than the logic circuit of figure 1. Applicant has failed to describe or even suggest any other embodiments that could deliver the described advantages over the prior art circuit and method for generating a pulse. Every disclosed embodiment includes the passgate circuit for generating the pulse signal. The pass gate

is clearly a critical or essential element that is required to perform the above steps as described in connection to figures 1 and 3.

In the remarks, applicant argued in substance that:

1. The broad language in the specification at col. 8, lines 63-65 expressly states that the above disclosure is illustrative only, and changes may be made in detail, and yet remain within the broad principles of the invention. Therefore, a pass gate is not critical element of the invention.

2. Figure 3 merely illustrates one embodiment of the signal generating circuit. Figure 3 is a particular embodiment of the invention, it is not the invention itself, but an example of the present invention. Therefore, a pass gate is not critical element of the invention.

The examiner disagrees with applicant's contentions. The pass gate is clearly a critical or essential element of applicant's invention. Applicant's invention, as disclosed in the specification, is described as a circuit including a pass gate for generating a pulse with minimal delay. The Abstract describes the invention only as a circuit including a pass gate. Indeed, every sentence in the Abstract except the last one includes at least one recitation of the word "passgate". The entire Summary Of The Invention discloses the invention in terms of a passgate circuit. The word "passgate" appears in the summary thirteen times, in nearly every sentence. The Detailed Description Of The Invention also discloses the invention in terms of a passgate circuit. Every embodiment disclosed in the specification includes the passgate circuit. The embodiment of figure 3 clearly includes the passgate circuit. The alternative embodiment disclosed at column 5,

lines 5-16 includes the passgate circuit and passgate control circuitry 156. The other disclosed embodiments describe using the passgate circuit of figure 3 in a memory device of a computer system as shown with figures 5-6 and at column 6, lines 40-42. No other methods of performing the above steps and no other devices other than passgates are described in the specification for generating the disclosed pulse. In addition, applicant has distinguished the invention over the described prior art method and circuitry for generating a pulse by using a pass gate rather than the logic gate (NAND 40) in the circuit of figure 1. Applicant describes the advantages of using a pass gate over the prior art circuitry at column 6, lines 22-39. This is clear evidence that the passgate is a critical element because applicant's pulse generating circuit generates the prior art pulse using a passgate circuit rather than the logic circuit of figure 1. Applicant has failed to describe or even suggest any other device that could deliver the described advantages over the prior art circuit and method of figures 1 and 2. The broad language in the specification at col. 8, lines 63-65 fails to describe or even suggest any other device that could deliver the described advantages over the prior art pulse generating circuit. In addition, applicant has failed to describe or even suggest any other embodiments that could deliver the described advantages over the prior art circuit and method for generating a pulse. The passgate is clearly a critical or essential element of applicant's invention and distinguishes applicant's invention over the prior art pulse generator of figures 1 and 2.

9. Claims 53-72 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant's amendment does not meet 1.173(c) which requires an explanation of the support in the disclosure for new claims. See MPEP 1453. The examiner was not able to find support in the specification for new claims 53-72. Particularly the recitations of the transfer gate and measuring the delay time or time period in claims 64-66 and 68-72. The burden remains on applicant to provide an explanation of support in the disclosure for new claims 53-72.

10. Claims 58 and 61-72 are rejected under 35 U.S.C. 251 as not being for the same invention as that disclosed as being the invention in the original patent. The specification describes the use of a pass gate to perform the steps of transferring and blocking the trigger signal from an input node to an output node, coupling and decoupling/deactivating the input node to the output node with figure 3, at column 4, lines 25-40 and at column 6, lines 29-39. No other methods of performing the above steps are described or enabled in the specification. The Abstract describes the invention only as a circuit including a pass gate. Indeed, every sentence in the Abstract except the last one includes at least one recitation of the word "passgate". The entire Summary Of The Invention discloses the invention in terms of a passgate circuit. The word "passgate" appears in the summary thirteen times, in nearly every sentence. The Detailed Description Of The Invention also discloses the invention in terms of a passgate circuit. Every embodiment disclosed in the specification includes the passgate circuit. The embodiment of figure 3 clearly includes the passgate circuit. The alternative embodiment disclosed at column 5, lines 5-16 includes the passgate circuit and

passgate control circuitry 156. The other disclosed embodiments describe using the passgate circuit of figure 3 in a memory device of a computer system as shown with figures 5-6 and at column 6, lines 40-42. No other methods of performing the above steps and no other devices other than passgates are described in the specification for generating the disclosed pulse. In addition, applicant has distinguished the invention over the described prior art method by using a pass gate rather than the logic gate NAND 40) in the circuit of figure 1 because it introduces less delay and therefore is faster than the prior art circuitry. Applicant describes the advantages of using a pass gate over the prior art circuitry at column 6, lines 29-39. This is clear evidence that the passgate is a critical part of applicant's invention because applicant's pulse generating circuit generates the prior art pulse using a passgate circuit rather than the logic circuit of figure 1. Applicant has failed to describe or even suggest any other device that could deliver the described advantages over the prior art circuit and method of figures 1 and 2. In addition, applicant has failed to describe or even suggest any other embodiments that could deliver the described generated pulse of figure 4 using a device other than a passgate. The passgate is clearly a critical or essential part of applicant's pulse generating invention and distinguishes applicant's invention over the prior art pulse generator of figures 1 and 2. Furthermore, applicant has provided no circuit or device for pass gate 120 of the specification. Pass gate 120 appears merely as an oval in figure 3 and the pass gate is defined in terms of the inputs and output. Any device or circuit having the disclosed inputs and output reads on the defined pass gate. Therefore, applicant's specification is completely lacking any description of a transfer gate. In

addition, applicant's specification is completely lacking any description of measuring the claimed time periods, measuring the claimed delay times, and generating the pulse of figure 4 with anything other than the described passgate circuit. Claims 58 and 61-72 are clearly directed to a different invention from the one disclosed in the specification and are not proper reissue claims under 35 U.S.C. 251. See MPEP 1412.01.

In the remarks, applicant argued in substance that:

1. Figure 3 merely illustrates one embodiment of the signal generating circuit. Figure 3 is a particular embodiment of the invention, it is not the invention itself, but an example of the present invention. The specification enables claims 58 and 61-72.

The examiner disagrees with applicant's contentions. Claims 58 and 61-72 are clearly directed to a different invention from the one disclosed in the specification and are not proper reissue claims under 35 U.S.C. 251. The specification does not disclose and/or enable the inventions recited in claims 58 and 61-72 as described in the above rejection.

11. Claims 58 and 63-64 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art.

Per claim 58:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. transferring the trigger signal from an input node (node 20/CLK) to an output node (node 60/IOPU) with figure 2 and at column 1, lines 40-60;

3. propagating the trigger signal through a delay circuit with delay circuit 34 and delayed clock IDCLK of figure 1 and at column 1, lines 43-46;

4. blocking the trigger signal and discharging the output node with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35. Figure 2 shows the output pulse at IOPU. The pulse ends with a low signal. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged to 0 volts as shown with IOPU of figure 2.

Per claim 63:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. coupling the input node (node 20/CLK) to an output node (node 60/IOPU) at which the pulse is provided with figure 1 and at column 1, lines 40-60;

3. decoupling the input node from the output node after a period of time with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35;

4. discharging the output node to a first state with the output pulse at IOPU. The pulse ends with a low signal. The prior art describes that the first state is the low state with CLK of figure 2 and at column 2, lines 7-14. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged to 0 volts as shown with IOPU of figure 2.

Per claim 64:

The prior art describes a transfer gate with NAND gate 40 of figure 1.

12. Claims 61-62, 67-68 and 71-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art.

Per claims 61 and 67:

The admitted prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal.

Per claim 62:

Precharging a node to a desired voltage is well known in the data processing art, particularly in the memory art, and it would have been obvious for one of ordinary skill in the art to precharge the output node to a desired voltage level.

Per claim 68:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. coupling the input node (node 20/CLK) to an output node (node 60/IOPU) at which the pulse is provided through a transfer gate (NAND gate 40) with figure 1 and at column 1, lines 40-60;

3. generating a deactivation signal (IDCLK) by delaying the trigger signal and deactivating the transfer gate with delay circuit 34 and delayed clock IDCLK of figure 1, at column 1, lines 43-46, with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35.

B) The claims seem to differ from the prior art in that the prior art fails to explicitly teach coupling the output node to ground to change the voltage level as claimed.

C) However, the prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal.

Per claims 71-72:

The admitted prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal. Precharging a node to a desired voltage is well known in the

data processing art, particularly in the memory art, and it would have been obvious for one of ordinary skill in the art to precharge the output node to a desired voltage level.

13. Applicant's arguments filed on March 26, 2003 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. Claim 58 does not teach blocking the trigger signal from the input node to the output node.

B. Claim 63 does not teach decoupling the input node from the output node after the period of time has elapsed and discharging the output node to the first state.

C. Claim 68 fails to teach or suggest deactivating the transfer gate in response to the generation of the deactivation signal to decouple the input node from the output node and coupling the output node to ground in response to the generation of the deactivation signal to change the voltage level of the output node to a voltage representative of the second state.

14. As to point A, the examiner disagrees with applicant's contention. NAND gate 40 clearly blocks the trigger signal (CLK) from the input node 20 to the output node 60 when signal IDCLK transitions from high to low as shown in figure 2 and at column 2, lines 27-59. Since gate 40 is a NAND gate, the trigger signal is inverted from a high value to a low value when it propagates through gate 40. However, it still passes through the gate. When IDCLK falls to a low value, the output of gate 40 will be a high

value regardless of the value of the trigger signal. The trigger signal is blocked from passing to the output by gate 40 and the pulse ends. The prior art uses the delay of devices 32 and 34 to set the length of the pulse signal. The pulse is ended and the trigger signal is blocked when CLK propagates through inverter 32 and delay 34 and the signal IDCLK falls to a low value.

As to point B, the examiner disagrees with applicant's contentions. NAND gate 40 clearly decouples the input node 20 from the output node 60 when signal IDCLK transitions from high to low as shown in figure 2 and at column 2, lines 27-59. Since gate 40 is a NAND gate, the trigger signal is inverted from a high value to a low value when it propagates through gate 40. However, it still passes through the gate. When IDCLK falls to a low value, the output of gate 40 will be a high value regardless of the value of the trigger signal and the output node is held at a low value. The trigger signal is decoupled from the output node by gate 40 and the pulse ends. The prior art uses the delay of devices 32 and 34 to set the length of the pulse signal. The pulse is ended and the output node is decoupled from the trigger signal (input) when CLK propagates through inverter 32 and delay 34 and the signal IDCLK falls to a low value. Regarding discharging the output node to the first state, the pulse ends with transitioning the output node from a high value to a low value signal. The prior art describes that the first state is the low state with CLK of figure 2 and at column 2, lines 7-14. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged from the high value to 0 volts as shown with IOPU of figure 2.

As to point C, the examiner disagrees with applicant's contentions. Transfer gate NAND 40 clearly decouples the input node 20 from the output node 60 when deactivation signal IDCLK transitions from high to low as shown in figure 2 and at column 2, lines 27-59. Since gate 40 is a NAND gate, the trigger signal is inverted from a high value to a low value when it propagates through transfer gate 40. However, it still passes through the transfer gate. When deactivation signal IDCLK falls to a low value, the output of transfer gate 40 will be a high value regardless of the value of the trigger signal and the output node is held at a low value. The trigger signal is decoupled from the output node by transfer gate 40 and the pulse ends. The prior art uses the delay of devices 32 and 34 to set the length of the pulse signal. The pulse is ended and the output node is decoupled from the trigger signal (input) when CLK propagates through inverter 32 and delay 34 and the deactivation signal IDCLK falls to a low value. Regarding discharging the output node to the first state, the pulse ends with transitioning the output node from a high value to a low value signal. The prior art describes that the first state is the low state with CLK of figure 2 and at column 2, lines 7-14. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged from the high value to 0 volts as shown with IOPU of figure 2. It is well known in the data processing art that 0 volts normally corresponds to ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal.

15. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2185